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Effects of Aspect Ratio in Moulded Packaging Considering Fluid/Structure Interaction: A CFD Modelling Approach

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ABSTRACT

The fluid/structure interaction (FSI) investigations of stacked chip in encapsulation process of moulded underfill packaging using the two-way Coupling method with ANSYS Fluent and ANSYS Structural solvers are presented. The FSI study is executed with different aspect ratio of stacked chip on the mould filling during the encapsulation process. The simulation results in the FSI study is well validated with experimental setup. The epoxy moulding compound (EMC) and structure (chip) interaction is analyzed for better understanding the FSI phenomenon.Von Mises stresses experienced by the chip also be monitored for risk of chip cracking. The proposed analysis is anticipated to be a recommendation in the chip design and improvement of 3D integration packages.

Keywords: Air void; Deformation; Moulded packaging; Stacked chip; Aspect ratio.

NOMENCLATURE

A_1, A_2	pre-exponential factors	T_b	temperature-fitted constant
B	exponential-fitted constant		
C_1,C_2	fitting constant	α	conversion of reaction
C_p	specific heat	α_{gel}	degree of cure at gel
E_1, E_2	activation energies	ΔH	exothermic heat of polymerization
k	thermal conductivity	η	viscosity
K_1,K_2	rate parameters described by an Arrhenius temperature dependency	n	power law index
		p	pressure
m_1,m_2	constants for the reaction order	η_0	zero shear rate viscosity
T	Temperature	τ	shear stress

1. INTRODUCTION

Flip chip technology has become a promising method in electronics packaging due to its high electrical performance and high interconnect density. However, the reliability of the electronic package still become one of the critical issues that restrict the usage of this technology. Therefore, encapsulation and underfill process are introduced to enhance the electronics package reliability. The chip is placed in the mould cavity during the encapsulation process. Then, the IC microchip is being capsulated with epoxy moulding compound (EMC) via the transfer moulding process to protect from physical damage and hazardous environment. The defects (i.e interconnector fracture, warpage, critical

displacement or deformation of chip and bump and void formation) and electronics package reliability reduction could be caused by the improper of the encapsulation process. Therefore, the understanding of the process mechanism will help microelectronic industry and scholars to accomplish their goals in the 3D electronic packaging.

The moulded flip–chip packaging are achieved by combining the underfill and encapsulation processes into a single process. The encapsulant flows beneath the structure (IC chip) and moves straight pass the solder bump during the underfill process. Meanwhile, in the encapsulation process, the EMC moves on top and bottom of the chip and encloses the chip simultaneously. The viscous fluid from the EMC causing the stress to the chip that may bring unintended defects. During this process, interaction between the EMC and structures happens. However, it is difficult to observe experimentally for the fluid/structure interaction (FSI) problems. So, a simulation modelling technique may be used for the analysis of the FSI problems. Previous studies have reported numerous numerical methods have been applied in predicting underfill flow, including finite-element method (FEM) (Wu *et al*., 1996, Haagh and Van De Vosse, 1998) finite difference method (FDM) (Abdullah *et al*., 2008, Abdullah *et al*., 2010) and finite volume method (FVM) (Khor *et al*., 2012, Ong *et al*. 2012, D. Ramdan *et al*., 2012). Numerous researchers have provided in-depth analysis on the use of the FEM and FVM that combined with MpCCI software for structure and fluid flow analysis (Gatzhammer *et al*., 2010, Yigit *et al*., 2008, Dadan Ramdan *et al*., 2012).

Zheng *et al*. (2008) also conducted two-dimensional underfill flow modelling to study the effect of large dies with nonuniform bump arrangements with two different flow models. Moreover, Wan *et al*. (2009) conducted another numerical study on underfill flow front predictions and compared their results with the experimental work of Nguyen *et al*. (1999). They used power law distribution to represent the non-Newtonian fluid behaviour of underfill epoxy. Khor *et al*. (2010) also investigated three-dimensional conventional underfill flow modelling to study the effect of solder bump pattern on the encapsulant flow by using FV-based software FLUENT. They found out that solder bump pattern in the flip chip underfill had a vital effect on velocity and filling time. The full array package which presence the highest number of solder bump consumed longer filling time for the underfill process.

In another major study, Teng and Hwang (2008) combined of the Mouldex3D-RIM software and commercial finite element (FE)-based ANSYS to perform structural analysis on encapsulation of the TQFP process. They were utilized generated fluid flow data from the Mouldex3D-RIM and transferred to ANSYS for structural calculation. Their results showed the lead frame that imposed to unstable forces was attribute to unstable filling.

The advance simulation method in FSI have been applied in various application such as pressure-swirl atomizers (Ayani *et al*., 2010), solid-liquid interaction (Mirzaii and Passandideh-Fard, 2011), solid objects motion (Mirzaii and Passandideh-Fard, 2012) and liquid sloshing in containers (Elahi *et al*., 2015). Recently, Nordanger *et al*., (2016) studied the effect of regularity and high polynomial orders, resolution sensitivity, mesh quality and stiffness distribution for flow past a circular cylinder in coupled FSI simulation. They found out that computational cost is similar although the mesh distribution is different and quadratic or cubic elements are better with reasonably fine grid.

In the current research, two way FSI method is applied on the moulded package to study deformation of the integrated circuit (IC) chip during the encapsulation process. The ANSYS is used to carry out the FSI simulation model of the package. The non-Newtonian behaviour and the curing characteristic of the EMC are described by the Castro-Macosko and Kamal models. The volume of fluid (VOF) method is used to track the melt front advancement in the FLUENT solver. The chip is defined as FSI structures in Structural. The ANSYS system coupling is employed to connect the FLUENT and Structural solvers by transferring the solution between the two solvers. This technique helps to visualize the actual interaction among the EMC and the chip in moulded packaging for different aspect ratios.

2. PROBLEM DESCRIPTION

Thinned silicon chip has been applied to achieve the 3D packaging and compress characteristics of IC packages. Nevertheless, the thinned silicon chip reliability is reduced during the subsequent electronic packaging process. Therefore, the interaction between structure (IC chip) and fluid (EMC) may cause high stress concentration and deformation on the chip. Consequently, the IC chip quality and reliability are diminishes. The FSI occurrence is hard to recognize in the real IC encapsulation process. Hence, a clear scaled-up mould (Fig. 1) with four variation chip aspect ratio was produced to deliver better understanding and visualization. The current work was also extended to examine the influence of chip aspect ratio on the stress concentration and deformation. Therefore, four different silicon chip aspect ratio (1.5, 2.0, 2.5, 3.0) were considered in the FSI simulation.

3. GOVERNING EQUATIONS

The governing equations describing the fluid flow are conservation equations of mass, momentum and energy. The EMC and air are assumed incompressible and laminar. The conservation of mass is defined as:

$$\frac{\partial \rho}{\partial t} + \frac{\partial}{\partial x_i}(\rho u_i) = 0 \quad (1)$$

The conservation of momentum is described by:

$$\frac{\partial}{\partial t}(\rho u_i) + \frac{\partial}{\partial x_i}(\rho u_i u_j) = -\frac{\partial P}{\partial x_i} + \frac{\partial \pi_{ij}}{\partial x_j} + \rho g_i + F_i \quad (2)$$

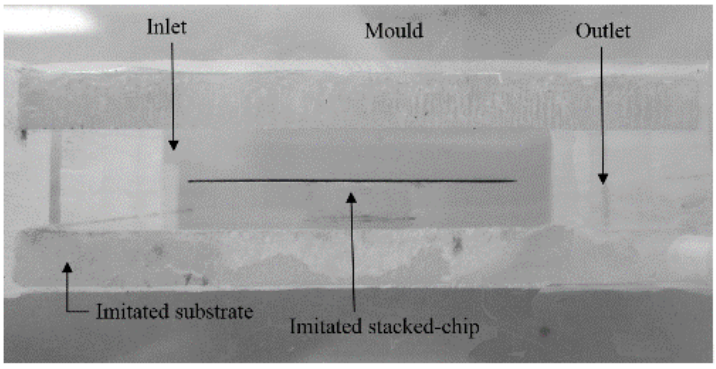


Fig. 1. Stacked chip arrangement in mould cavity.

The conservation of energy can be expressed as:

$$\frac{\partial}{\partial t}(\rho h) + \frac{\partial}{\partial x_i}(\rho u_i h) = \frac{\partial}{\partial x_j}\left(k\frac{\partial \pi_{ij}}{\partial x_i}\right) + \eta\dot{\gamma} \quad (3)$$

where, P is the fluid pressure, πij is the stress tensor and gi and Fi are the gravitational acceleration and external body force in the i direction, respectively, T is the temperature, k is the thermal conductivity, η is the viscosity and $\dot{\gamma}$ is the shear rate.

In this study, the volume of fluid (VOF) method is used to capture the flow front advancement between the EMC and air (Hirt and Nichols, 1981). The method which use a scalar function α, where 0 < α< 1, to illustrate the interface profile. If the value of α is set to 1, the cell is occupy of a fully liquid phase meanwhile when the α is set to zero, the cell consist only a gas phase. The VOF can be defined as

$$\frac{\partial}{\partial t} + (\alpha\rho) + \nabla.(\alpha\rho\vec{v}) = 0 \quad (4)$$

Castro–Macosko model (Castro and Macosko, 1980) and Kamal models (Kamal and Sourour, 1973) were utilized to describe the non-Newtonian behaviour and curing kinetics of the epoxy moulding compound (EMC) EME 6300HN (Nguyen *et al.*, 2000).This viscosity model has combined the dependence on curing, strain rate and temperature. It can be expressed as:

$$\eta = \frac{\eta_o}{1 + \left(\frac{\eta_o \gamma}{\tau^*}\right)^{1-n}}\left(\frac{\alpha_g}{\alpha_g - d\alpha/dt}\right)^{c_1 + c_2\alpha} \quad (5)$$

$$\eta_o = B \exp\left(\frac{T_b}{T}\right) \quad (6)$$

where η is the viscosity at temperature T, γ is the shear rate, α is the degree of cure,ηo is the zero shear viscosity, n is the power law index, τ* is a shear constant, αg is the degree of cure at gel point and C1, C2, B, and Tb are the fitted constants.

The curing model is described as:

$$\frac{d\alpha}{dt} = (k_1 + k_2\alpha^{m_1})(1-\alpha)^m, \quad (7)$$

$$k_1 = A_1 \exp\left(-\frac{E_1}{T}\right), k_2 = A_2 \exp\left(-\frac{E_2}{T}\right) \quad (8)$$

where E1 and E2 are the activation energies, A1 and A2 are the Arrhenius pre-exponential factors, m1 and m2 are the reaction orders and T is the absolute temperature. These viscosity and curing models have been used by many scholars (Yang *et al.*, 1997, Chang *et al.*, 2004, Khor *et al.*, 2012, D. Ramdan *et al.*, 2012, Shen *et al.*, 2004). Table 1 lists the material properties of EME 6300HN.

Table 1 Details of package geometry

Case	1	2	3	4
aspect ratio	a/b=1.5	a/b=2.0	a/b=2.5	a/b=3.0

The EMC rate of conversion can be modelled as:

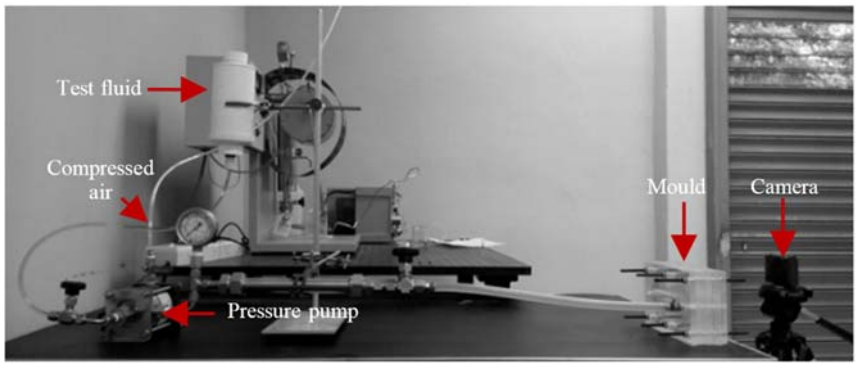
$$\alpha = \left(\frac{\Delta H(t)}{\Delta H_{total}}\right) \quad (7)$$

where α is the EMC degree of cure, ΔH(t) is the heat generated by EMC at time t, ΔH_{total} is the total heat generation at the complete EMC cure.

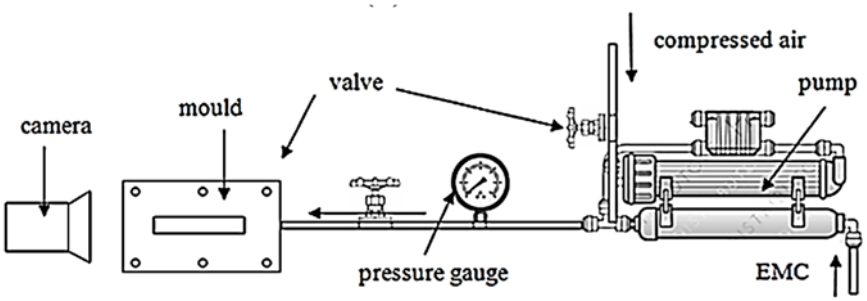
4. EXPERIMENT SETUP

An experiment was executed with the purpose of proving the feasibility of simulation by comparing it to the results of experiment. For the experiment setup, a transparent mould assembly was designed to give clear visualization accordingly as depicted in Fig. 2. The dimension of mould cavity is 8.0 cm×4.0 cm×1.6 cm and the thickness of substrate is 0.45cm. Fig. 3 depicted the chips placed on a substrate in the mould cavity. In order to provide clear view of FSI, transparent plastic material were used to make the stacked-chip.

A test fluid with density at 1072 kg m−3 and viscosity at 4.0 Pa.s was used in the experiment as the encapsulant material. The inlet pressure was measured and setup consistently at1.0 MPa by the pressure gauge. A camera was used to capture the encapsulation process and was placed in front of the mould. In this experimental work, temperature effect was not considered because the interaction between the structures and the fluid is the only focused problem.



(a) Actual



(b) Schematic diagram

Fig. 2. (a) Actual diagram and (b) schematics of the experimental setup.

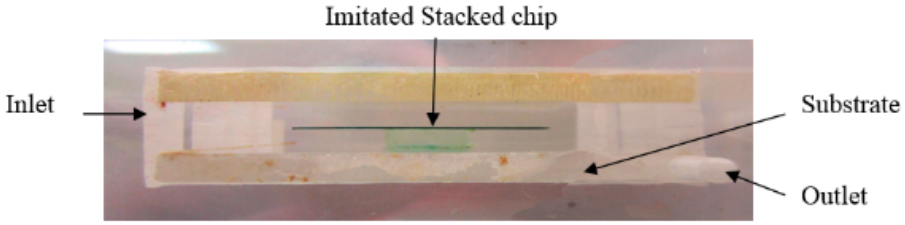


Fig. 3. Stacked chip arrangement in mould cavity for case 1.

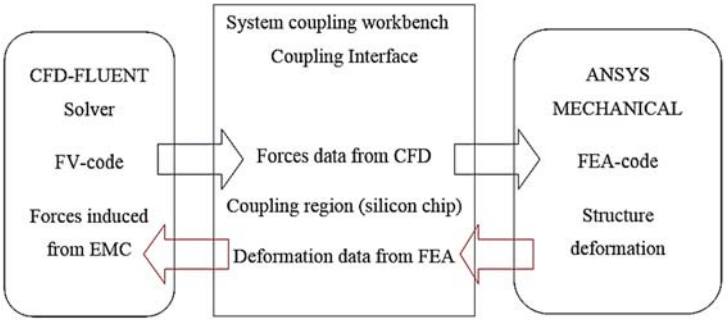


Fig. 4. Two way system coupling technique.

5. FSI SIMULATION MODELLING

In the current work, the FSI technique is conducted by coupling of FLUENT and Transient Structural, which are linked by System Coupling workbench. Fig. 4 illustrated the data exchange from FLUENT and Structural by using the two ways coupling technique. During FSI analysis, actual solution were transmitted between the two solvers. The pressure produced from the FLUENT solver were transmitted to Structural solver by System Coupling workbench. Therefore, the calculation for deformation were done

simultaneously. The deformation of structure in Structural solver return the data back to the FLUENT. The FLUENT solver was utilized to model the EMC that filled into the cavity. The Transient Structural was utilized to compute the stress and displacement during the encapsulation process.

5.1. Geometrical Modelling

Four cases consisted of two-stacked chips with 1.5, 2.0, 2.5, 3.0 aspect ratio were considered in this study, as shown by Table 2. ANSYS ICEM was utilised to generate the geometrical modelling and meshing. The ANSYS FLUENT 14.0, was utilized to model the fluid flow and solve the governing equation of the EMC flow field. Four type of the flip chip with different aspect ratio namely case 1, 2, 3 and 4 as shown in Fig. 3. A moulded IC package, as depicted in Figs. 4-5, is designed by ANSYS Design Modeler ANSYS ICEM was the pre-processing tool utilized for meshing and boundary condition setting. A total of 470,564 hexahedral elements were created for each of the model according to the dimensions of the package, as shown in Table 2.

Table 2 EMC material properties used in FLUENT simulation

Castro-Macosko model parameters	
B (Pa.s)	$1.624e^{-7}$
T_b (K)	11620
C_1	3.338
C_2	0.2824
α_g	0.4447
Kamal model parameters	
m_1	0.4925
m_2	1.117
A_1 (s−1)	29730
A_2 (s−1)	$4.836e^{6}$
E_1(k)	25330
E_2(k)	8443

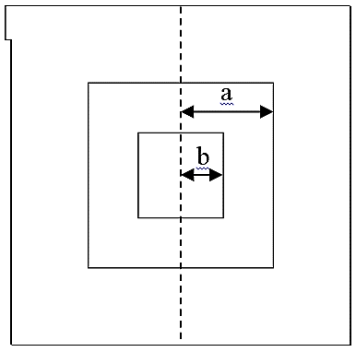


Fig. 5. Moulded package.

In FLUENT 14.0, the fluid and air are defined as two different phases. During the encapsulation process, Volume of fluid (VOF) equations solved the modelling between two phases. The VOF method was applied in order to capture the EMC flow front.

In the analysis, the non-Newtonian fluid flow is modelled by the Castro-Macosko and Kamal models. The non-Newtonian models were written in c++ language and imported into fluent by user defined function (UDF). Table 3 summarized the EMC material properties for the current study.

Table 3 Properties used in the FSI analysis

	chip	spacer
Elastic modulus, E (GPa)	1.57	2.7
Poisson ratio, v	0.37	0.375
Solid density, p_s (kg/m^3)	1180	1170

In the mould setup, a constant 1.0 MPa inlet pressure was used in the present study. Preheats temperature was set to 90°C and the mould temperature (T_w) was set to 150°C. For the FSI calculations, the dynamic mesh setting is enable. The volume fraction, energy equations and momentum was applied with the second-order upwind scheme. A COUPLED scheme is utilized for pressure-velocity computation. The COUPLED algorithm is used for exchange data between fluid and structural solver. Time dependent and implicit VOF scheme are used for the volume fraction in every time step. The volume fractions of the encapsulant material and air phase are assigned as one and zero respectively. In VOF method, implicit body force treatment is applied to improve solution convergence. The time step of 0.001 s is used for the simulation. Furthermore, the surface tension model and the wall adhesion model are enabled to take into account the effect of surface tension along the interface of two fluids and the contact angle that the fluid makes with the wall. For one case of simulation, it took approximately 16 hour to complete the calculation by using an Intel Core i7-4790, 3.60GHZ, and 16GB of ram. Fig. 6 depicted the boundary conditions applied to the package.

The boundary conditions are listed in the following:

On wall boundary: u = v = w = 0 ; T = T_w, $\frac{\partial p}{\partial n} = 0$

On center Line: $\frac{\partial u}{\partial z} = \frac{\partial v}{\partial z} = \frac{\partial w}{\partial z} = \frac{\partial T}{\partial z} = 0$

On melt front: p=0

At Inlet Gate: $P=P_{inlet(x,y,z,t)}$; $T=T_{inlet}$

5.2 Structural Modelling

The present analysis solves the deformable structure of the IC chip .The structure is designed and meshed using the ANSYS Structural by following to the dimensions mentioned in Table 4. The hexahedral elements is used for the mesh production as depicted in Fig. 7. The fixed boundary condition was applied at the lowest part of the stacked chip. During the moulding process, the rigid stacked chip is clamped and fixed in the mould as illustrated in Fig. 8. Fluid/structure interaction (FSI) structure was set at the top of chip. Table 4 summarized the IC chip material properties and material assignment applied for analysis of the structure.

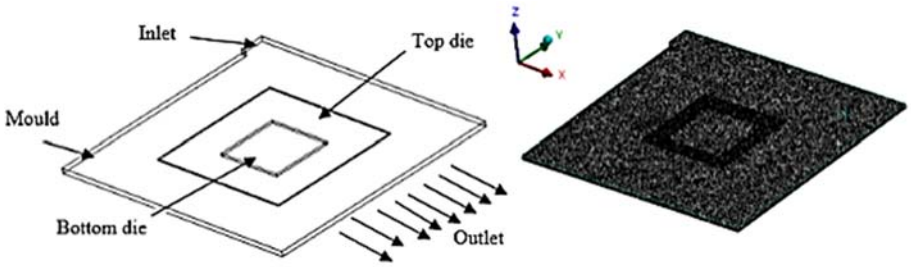


Fig. 6. Boundary conditions and meshed model of the imitated chip.

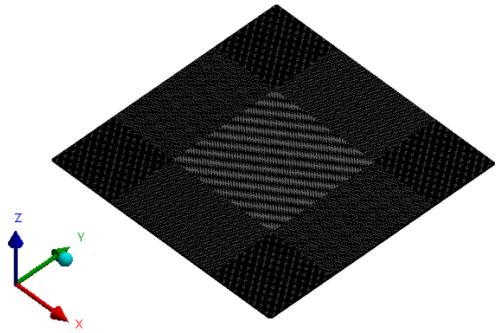


Fig. 7. Mesh model of chip.

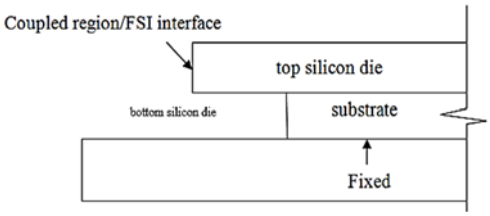


Fig. 8. Boundary condition for structural solver.

5.2 Grid Independence Test

The summary of grid independence test is presented in Table 4 which shows the percentage mold filling at various mesh sizes at 90% of filling time. Case 6 being the finest in grid size, the deviations in percentage filling volumes of cases 1, 2, 3, 4 and 5 from case 6 are tested. It is observed that, case 5 and case 6 are better with nominal deviation (0.48%) between them; thus, case 5 is chosen as the optimum in terms of accuracy and computational cost.

Table 4 Summary grid independence test

Case	Elements	Volume % at 90% of filling time	Deviation from case 6
1	81435	90.98	8.69
2	179997	89.05	6.76
3	264656	88.12	5.83
4	355202	86.88	4.39
5	470564	82.77	0.48
6	610536	82.29	0.00

6. RESULT AND DISCUSSION

There are limited literature on 3-D moulded IC packaging experimental data. Therefore, a moulded prototype were produced to validate the experimental with numerical results. Fig. 9 shown the comparison results between experimental and simulation for case 2. As shown in Fig. 10, the filling profile reported nearly identical pattern from both the experimental and simulation. The advantage of the simulation with FLUENT was verified as excellent for the flow during encapsulation process. Thus, the present modelling methodology give reliable predictions in encapsulation process.

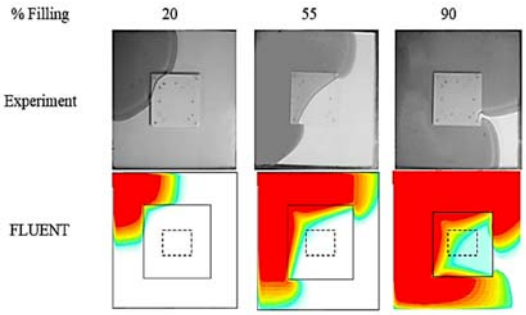


Fig. 9. Comparison between FLUENT and experimental results at different process times for case 2.

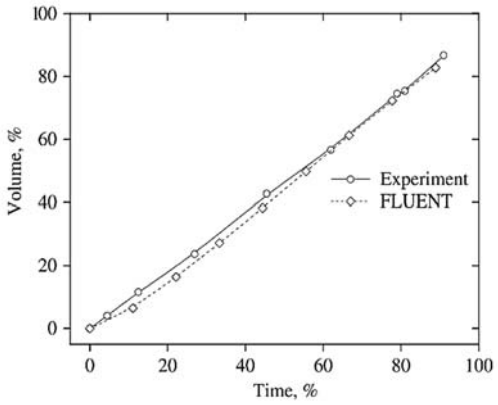


Fig. 10. Comparison of present simulation (FLUENT) and experimental data.

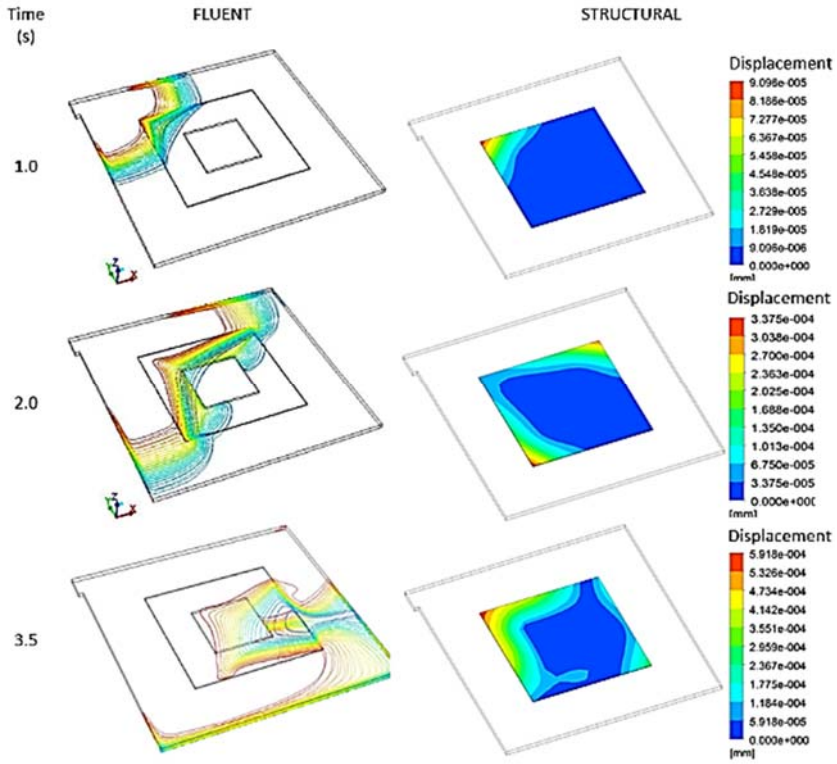


Fig. 11. Molded package chip deformation during encapsulation process for case 2.

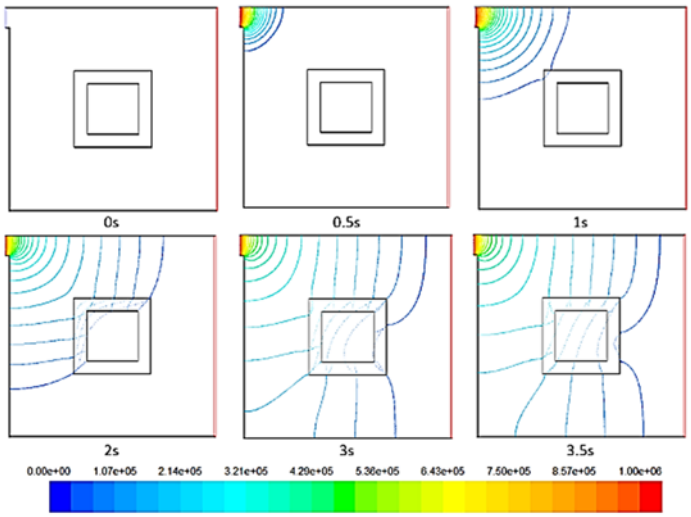


Fig. 12. Pressure distribution at different filling times (case 1).

6.1 Fluid Structure Interaction

Figure 11 shows the deformation of IC chip during encapsulation process. From the data in Fig. 11, the EMC start to flow into the mould at 0.5s. The deformation of chip at the edge region is caused by the interaction between fluid and chip. Further assessment showed that the EMC start to cover the chip when the filling time between 1s to 1.5s. The deformation is noticed at the edge of the chip, where the region has no spacer. However, the flow front advancement is clearly unstable or non-uniform during this phase. Lower resistance at top of chip caused the flow is much faster compared with the bottom of the chip. The force occur on the chip caused the flow front of EMC on the top and bottom chip become unstable. This occurrence may lead to the initial warpage once the encapsulation process is complete. The mould is almost filled at 2–3 s and deformation is detected on the chip near the outlet vent. The outcomes obtained shown that the concentration for the deformation on the chip is nearly at the inlet and outlet area. Furthermore, the void formation and variation of pressure on the chip

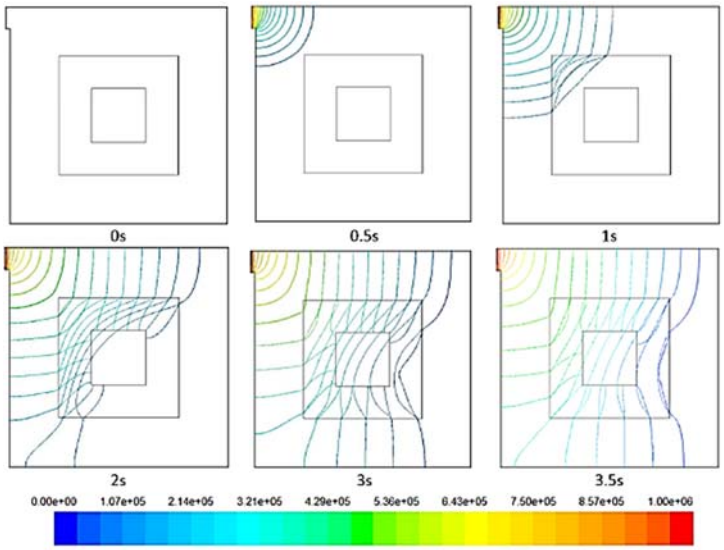


Fig. 13. Pressure distribution at different filling times (case 2).

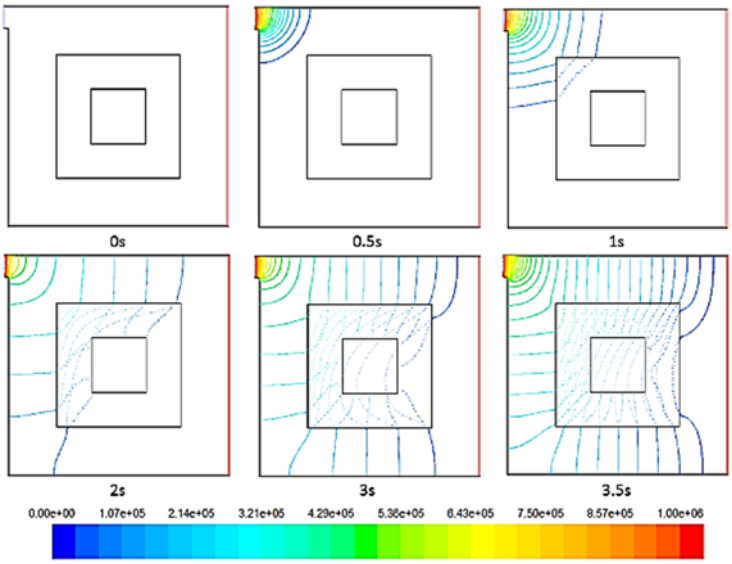


Fig. 14. Pressure distribution at different filling times (case 4).

could cause by the number of inlets and outlets (Khor *et al*., 2011). Consequently, the optimized design and position of the inlet gate could effectively minimize the void formation and enhance the package reliability.

Figures 12, 13 and 14 illustrate the pressure distribution at various filling times (case 1, 2, 4). The pressure is examined after the mould cavity is completely filled with EMC. In the study, the unstable EMC flow cause by the difference aspect ratio between bottom and top of chip is examined. The unstable pressure that is allocated on the chip surface caused by the unstable EMC flow. At the early phase (0.5 s), the pressure displays a consistent contour, particularly at the bottom and top of the chip. However, at 1-3 s, the pressure begins to be dispensed irregularly. The distributions of pressure on the chip are nearly identical when the mould is almost fully occupied by the EMC (3.5 s).
Figure 15 displays the velocity magnitude at various filling times (case 2). The flow through the narrow space between stacked chips had lower velocity compared to mould area.

6.2 Deformation

Different chip aspect ratio was studied on the deformation during the encapsulation process. The results obtained from the deformation measurements for points P1 to P4 at the chip are presented in Fig .16.

6.2.1 Filling Process

The chip maximum deformation was evaluated and analyzed for different aspects ratio during the

encapsulation process. The deformation is generated by the EMC fluid and chip interaction, the flow front stability and pressure difference. From the results, the crucial and critical deformation area was recognized; it appeared at the point P1 close to the inlet vent. Fig. 17 shows the effect of the aspect ratio on the chip at position P1.There is a clear trend of increasing when the aspect ratio increased from 1.5 to 3.0, and the deformation at P1 also increased progressively. However, when it reached at the peak point of deformation, the value of deformation at P1 fluctuates. For aspect ratio 2.5 and 3.0, the vibration of chip is clearly detected after the peak point. The chip began to vibrate after 0.8s until the process end at 3.5s. This phenomenon happen because of lack of support at the edge chip area and continuous flow of EMC. The hydrodynamic force on the structure increased as the aspect ratio is increased. As a result, deformation occur at the bottom and top of chip when the variation of force created by the non-uniform flow of EMC. Additionally, the continuous EMC fluid is fed into the cavity caused the fluctuation generated in the process. High stress on the chip is developed when the force on the structure is increased rapidly. It can thus be suggested that, the aspect ratio need to be controlled less than 2.0 to avoid this deformation fluctuation. Thus, package design, material selection and suitable controllable parameter are important to maintain quality and reduce defects.

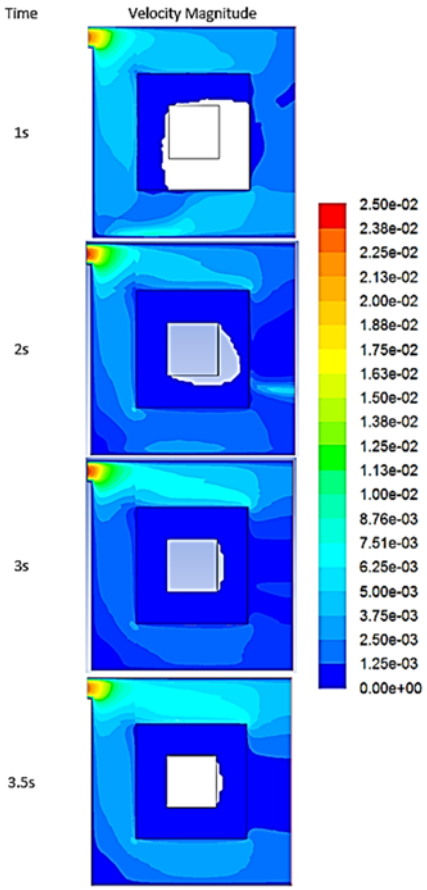


Fig. 15. Velocity vectors during encapsulation process for case 2 (unit: ms^{-1}).

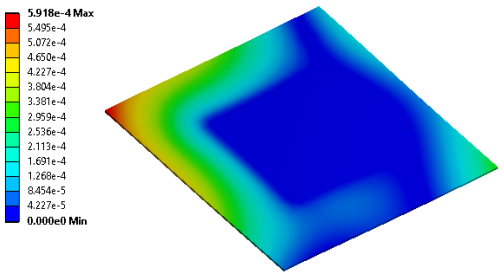


Fig. 16. Points P1 to P4 at different locations of the silicon die.

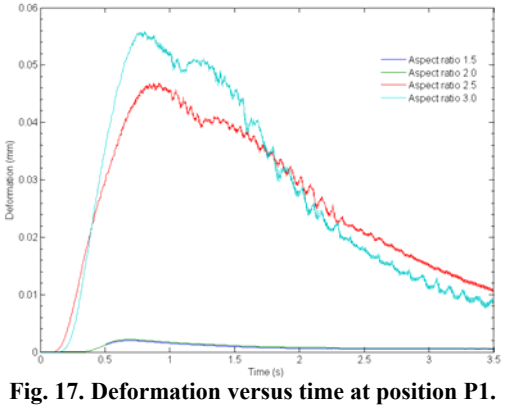


Fig. 17. Deformation versus time at position P1.

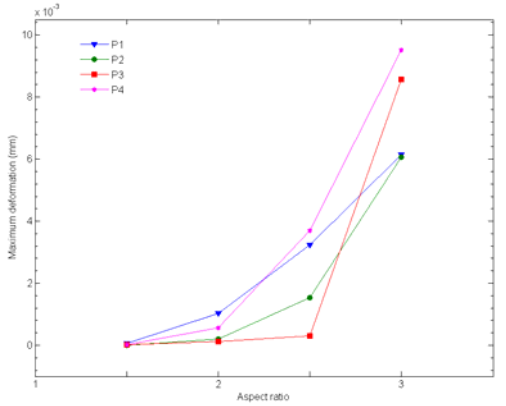


Fig. 18. Maximum deformations for different aspects ratio at selected positions P1, P2, P3, and P4 of the final filling stage.

6.2.2. Complete filling

The chip deformation at various chip aspects ratio was determined when the filling process is completed the filling. The current study illustrates that the chip deformation is directly proportional to aspect ratio. Fig. 18 depicted filling process for the critical deformation. The critical points P1 and P3 are analyzed and showed in Table 5

The deformation at two points (P1 and P3) are compared and presented in Table 5. The deformation percentage difference is computed as shown in Eq. (10).

$$\% \text{ of diff} = \left| \frac{\text{Point 1} - \text{Point 2}}{(\text{Point 1} + \text{Point 2})/2} \right| * 100 \qquad (10)$$

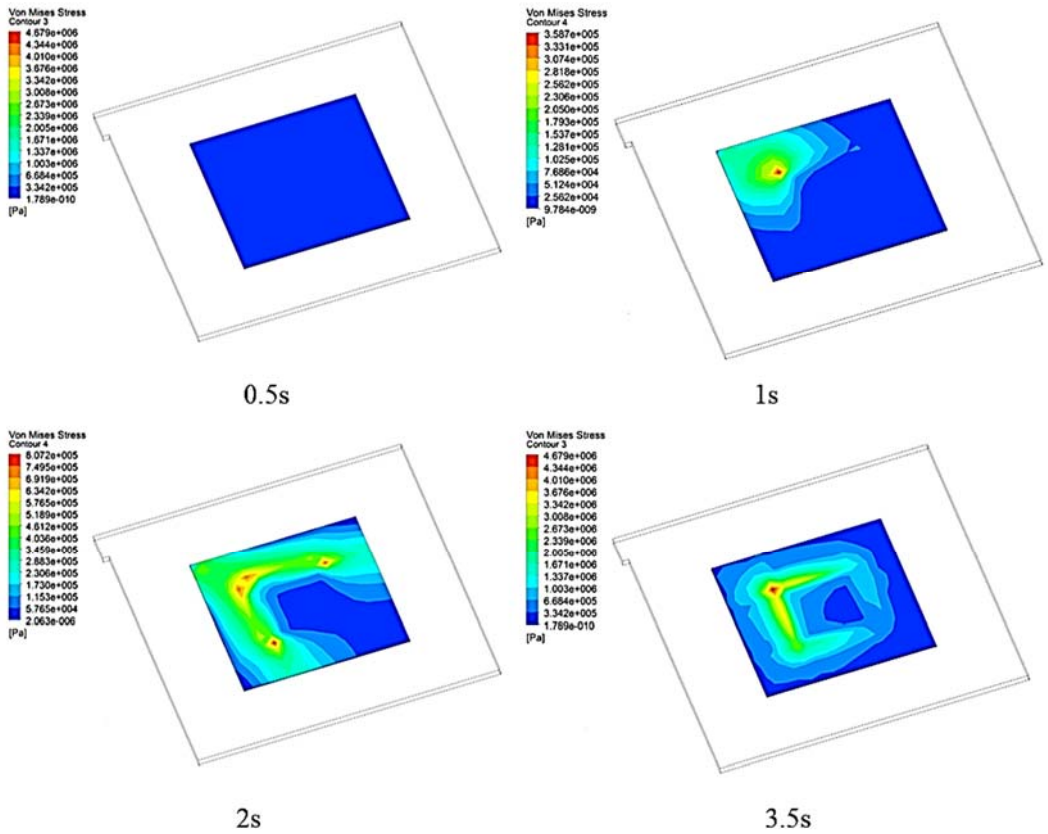


Fig. 19. Stress distribution on the silicon die during the encapsulation process from 0.5 s to 3.5 s of filling time (aspect ratio 2).

The percentage difference of deformation between the points P1 and P3 varied for different aspect ratios. The findings of this study indicate that non-symmetrical deformation behaviour occurred at P1 and P3. This could be caused by the non-uniform EMC during mould filling process. Furthermore, the deformation difference could be effected by the movement of chip during the interaction.

Table 5 Percentage difference for points (P1 and P3) at opposite positions for the final filling stage

Aspect ratio	Points		
	P1	P3	% Diff
1.5	5.43E-5	2.41E-5	77.04
2.0	1.04E-3	1.13E-4	160.86
2.5	3.23E-3	3.12E-4	164.78
3.0	6.14E-3	8.56E-3	33.04

6.3 Von Mises Stress Analysis

The stress on the chip were studied and recognized at the maximum stress region when the encapsulation process started. Fig. 19 shows the encapsulation process for stress distribution analysis (aspect ratio 2). The concentration of stress is discovered on the top of chip within 2–3.5 s. The pressure difference caused the stress to be concentrated on the top of the chip as discussed in Section 6.3.

Figure 20 shows the stress concentration for point P1 (Fig. 16). The stress are concentrated at point P1 compared to other points on the top chip, as stated in Section 6.2.1. As the aspect ratio is increased, the stress on point P1 is also increased and produced non-stop fluctuation on chip when aspect ratio 3.0 is applied.

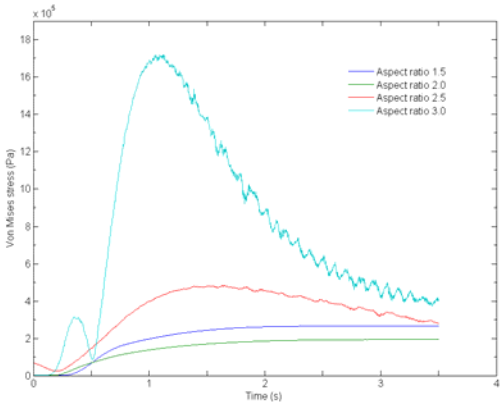


Fig. 20. Von Mises stress versus filling time at position P1.

Figure 21 depicted the maximum stresses on the chip for 'during filling stages'. Different aspect ratio was used to determine the maximum stresses during filling stages. The current research discovered that the maximum stress increases exponentially with the aspect ratio. The relationship between the stress and aspect ratio is presented in Fig. 21.

6.4 Void Formation

One of the critical issue in IC encapsulation is air void formation. The existence of void in an IC package may cause the popcorning problem during the reflow process (Gannamani and Pecht, 1996) and may affect the package reliability. In the current case, the incomplete filling is recognized according to the cell volume fraction. The highest possibility for formation of void occurred in the area with the volume fraction less than 0.5.

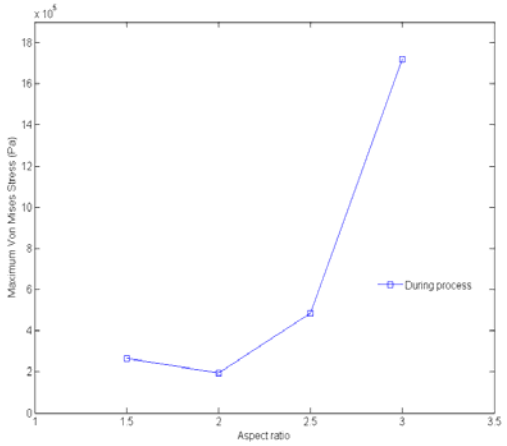


Fig. 21. Maximum von Mises stress versus aspect ratio at the ''during'' process stages.

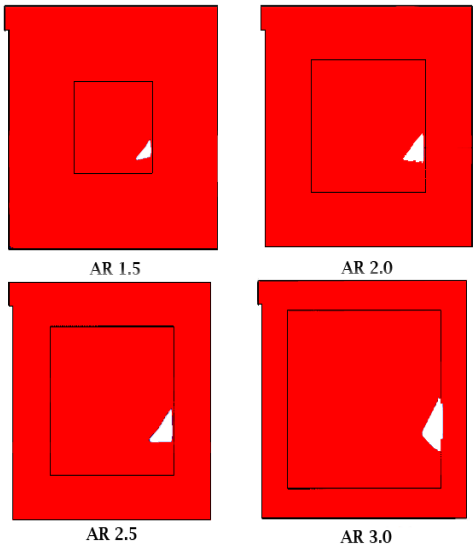


Fig. 22. Locations of the void concentration in the package for different aspect ratio.

An area with the volume fraction less than 0.5 (Nguyen *et al.*, 2000) had the highest chance of void formation. From the results in Fig. 22, the deformation around the edge of the chip and unsteady flow profile increased the formation of void in the IC package. Moreover, the studies show that the void is formed under IC chip which closer to the outlet vent. Fig. 23 plotted the incomplete filling percentage for various aspect ratio. The aspect ratio increment produced unsteady flow and instability during the encapsulation process (Fig. 24) that increase the possibility for void to generated during the encapsulation process. Hence, process optimization is needed to be performed by package engineer and designer in order to maintain quality and reliability.

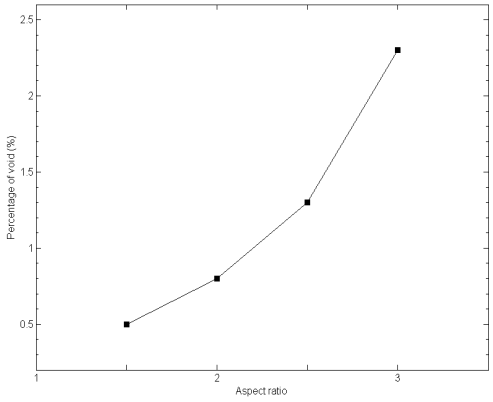


Fig. 23. Percentage of void formation for different aspect ratio.

In this study, the consideration of FSI in the encapsulation process showed that the aspect ratio caused the fluctuation phenomenon on the silicon die edge; the continuous fluctuation caused the disturbance and unstable flow (Fig. 24). Fig. 25 show the results of two IC chip with same aspect ratio at different distance between corners and the inlet. The result is evidently shown in the detailed view of deflection is only effects of the aspect ratio and is not effects of the distance between corners and the inlet. The deflection for both chip is same although the distance from inlet and corner is different.

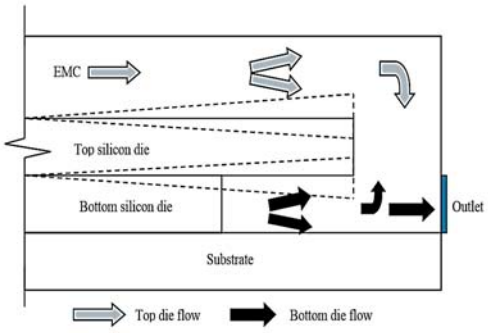


Fig. 24. Schematic of flow disturbance in the cavity.

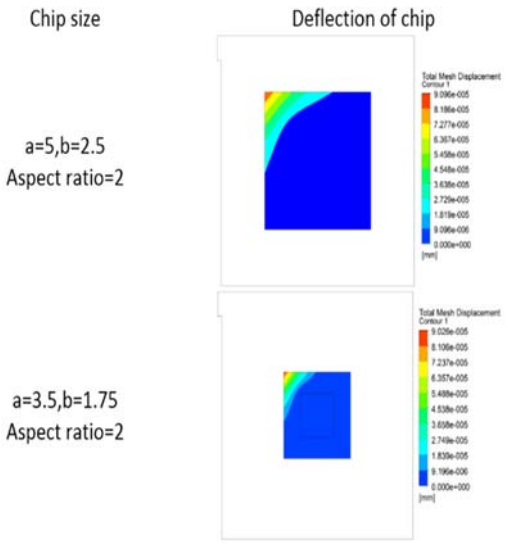


Fig. 25. Deflection of chip at different distance from corner and inlet (aspect ratio 2).

7. CONCLUSION

In this paper, the fluid/structure interaction analysis of increasing the aspect ratio in the moulded packaging are presented. Numerical modelling of the FLUENT and STRUCTURAL in simulating the encapsulation process produce reasonable predictions and contributed on the understanding the interaction between IC chip and EMC during the encapsulation process. This study has found that generally the stress distribution and deformation of the IC chip is increases exponentially when the aspect ratio is also increase. The findings of this study indicate that the edge of chip is subject to focal point of maximum stress and deformation. The aspects ratio of 2.5 and 3.0 produced the fluctuation and vibration occurrences on the chip. As a result, the flow become unbalanced and led to the void formation when the deformation fluctuation occurred. Taken together, these results suggest that the aspect ratio should be managed under 2.0 to avoid the chip to deform and fluctuate. The propose analysis and results in this study offered greater visualization and assist in the understanding of the FSI phenomenon.

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